

PRODUCTION OF SILICON SINGLE CRYSTAL HAVING LOW CRYSTAL DEFECT AND SILICON SINGLE CRYSTAL WAFER PRODUCED THEREWITH

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Abstract

PROBLEM TO BE SOLVED: To provide the silicon single crystal wafer which is grown by a CZ (Czochralski) method and in which no OSF(oxidation-induced stacking fault) ring is not caused at the time of subjecting the wafer to thermal oxidation treatment and any OSF ring nucleus is absent and also, in the whole surface of which no FPD (flow pattern defect, i.e., one of the grown-in defects) and no L/D(large dislocation) are present and further, which has an N1 (V) region expanded to the utmost, accordingly, an extremely low defect density and sufficient gettering capability, wherein the N1 (V) region is a neutral region located inside an OSF ring and between the OSF ring and an inner V (vacancy) region in a defect distribution diagram.

SOLUTION: This production involves pulling up a single crystal under conditions falling within an N1 (V) region inside an OSF ring in a defect distribution diagram drawn with F/G value and D value as the ordinate and abscissa, respectively, or at a 0.130 to 0.142 mm² / deg.C.min F/G value in the crystal center, wherein: F (mm/min) is a pulling-up rate of a single crystal in a CZ method; G (deg.C/mm) is an average temp. gradient value within the crystal in the direction of the pulling-up axis and in the range from the melting point of silicon to 1,400 deg.C; and D (mm) is the distance from the crystal center, up to the outer periphery of the crystal.

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(57)[SUMMARY] (Amended)

[SUBJECT] A silicon-single-crystal wafer with a gettering capability is provided. In the silicon-single-crystal wafer by which the growth was carried out by the CZ process, OSF ring is not generated at the time of a heat oxidation treatment, OSF ring nucleus does not exist, and FPD and L/D do not exist over the wafer

whole surface. It is the extremely low defect density for which N1 (V) area of this ring inner side was enlarged to the maximum.

[SOLUTION] Raising speed is set to F [mm/min] in the CZ process.

For the gradient degree mean value of crystal inside temperature in the raising axial direction to 1400 degrees C from the melting point of a silicon, when this is expressed with G [degree C/mm], f/G value is the vertical axis, and in the defective distribution diagram which made the horizontal axis D (distance from the crystal center to the periphery), it pulls up in N1 (V) area inside OSF ring.

Or F/G value is pulled up as 0.130 - 0.142 mm²/ degree-C *min at the crystal center.

[CLAIMS]

[CLAIM 1] A manufacturing method of the silicon single crystal, in which raising speed is set to F [mm/min] when the growth of the silicon single crystal is carried out by the Czochralski method.

When you express the mean value of the gradient degree of crystal inside temperature in the raising axial direction between 1400 degrees C from the melting point of a silicon by G [degrees C/mm], let distance D [mm] from the crystal center to the crystal periphery be the horizontal axis.

In the defective distribution diagram having shown the defective distribution, having used the value of F/G [mm²/degrees C * min] as the vertical axis, the boundary line of the V-rich area and N1 (V) area, and the boundary line of N1 (V) area and OSF ring area, a crystal is pulled up in N1 (V) area surrounded by this.

[CLAIM 2] A manufacturing method of the silicon single crystal described in Claim 1, in which at the crystal center, the above-mentioned value of F/G is pulled up as 0.130 - 0.142 mm²/ degree-C *min.

[CLAIM 3] A silicon-single-crystal wafer, which was produced from the silicon single crystal manufactured by the manufacturing method of Claim 1 or Claim 2.

[DETAILED DESCRIPTION OF INVENTION]

[0001]

[TECHNICAL FIELD] This invention relates to the manufacturing method and the silicon-single-crystal wafer of the silicon single crystal with few crystal defects.

[0002]

[PRIOR ART] In recent years, following the miniaturisation of the element accompanied by high integration of a semiconductor circuit, the quality demanded for the silicon single crystal produced by the Czochralski method (it abbreviates as the CZ process hereafter) used for a substrate has increased.

The defect of a single-crystal growth caused by worsening the oxide-film breakdown-voltage characteristic and the device characteristics especially called grown-in defects, such as FPD, LSTD, COP exist, and the reduction of the density and size is given importance.

[0003] To demonstrate these defects, first, the porosity type point defect called vacancy (it may abbreviate as V) received by the silicon single crystal, interstitial-Si, between lattices type silicon point defect (I in the following), about the factor affecting inclusion of each density, that generally known is demonstrated.

[0004] In a silicon single crystal, V area is an area with many cases like Vacancy, the recess generated from the insufficiency of silicon atom in other words, and a hole.

I area is the area with high mass of transition and the excessive silicon atom which are generated when the silicon atom exists excessively.

And between V area and I area, the neutral (Neutral may be abbreviated in the following as N) area without an atomic insufficiency and an atomic excess (low) will exist.

And, for (FPD, LSTD, COP etc. above-mentioned grown-in defects), finally, when V and I are in a supersaturated state, it generates.

If it is below saturation even when there is deviation of some atoms, it has turned out that it does not exist as a defect.

[0005] For the density of both of these point defects, raising speed of the crystal in the CZ process (growth rate), it is decided from the relationship with temperature-gradient G near the solid-liquid boundary surface in crystal.

In the limit neighborhood of V area and I area, OSF, existence of the defect of the shape of a ring so-called Oxidation Induced Stacking Fault) is confirmed.

[0006] If the defect of these crystal-growth reason is categorized, when a growth rate is comparatively as high-speed as the above around 0.6 mm/min, the reason for a hole in which porosity type point defects gathered, grown-in defects, such as FPD, LSTD, COP, exist with high density in the direction of the diameter throughout the crystal.

The area where these defect exists is called V-rich area (refer to diagram 4 (a)).

Moreover, when the growth rate is below 0.6 mm/min, in connection with a reduction of the growth rate, the above-mentioned OSF ring is generated from the periphery of the crystal.

The defect of L/D considered to be the transition loop cause by the outer side of this ring exists in low density. (abbreviation of the transition loop between Large Dislocation: lattices, LSEPD, LFPD etc)

The area where these defect exists is called I-rich area (refer to diagram 4 (b)). Furthermore, if the growth rate is made into a low speed 0.4 mm/min magnitude, OSF ring will condense and disappear at the center of the wafer, and the whole surface becomes an I-rich area (diagram 4 (c)).

[0007] Moreover, also FPD, LSTD, COP of the porosity causes recently called N (neutral) area to the outer side of the OSF ring in the intermediate of a V-rich area and an I-rich area, existence of the area where LSEPD of caused by transition loop and LFPD do not exist is discovered.

(Refer to Provisional Publication No. 8-330316).

This area is situated in the outer side of the OSF ring.

And, an oxygen precipitation heat treatment is given.

When the contrast of precipitate is confirmed by X-ray observation etc., there is almost no oxygen precipitate.

And, it is reported that it is the I-Si side which is not so rich that LSEPD and LFPD are formed (refer to diagram 3 (a)).

And, the temperature distribution in furnace of the raising machine is improved

for the neutral (N) area which exists in only a tiny part of the wafer in conventional CZ raising machine, and raising speed is adjusted.

F/G value (single crystal drawing speed is set to F[mm/min])

When setting to G[degrees C/mm] the mean value of the gradient degree of crystal inside temperature in the raising axial direction from the melting point of silicon to 1300 degrees C, if the ratio expressed with F/G is controlled over the whole wafer surface at 0.20 - 0.22 mm² / degree-C *min, it is proposed that it is possible to extend the N area over the wafer whole surface.

(Refer to diagram 3 (b)).

[0008]

[PROBLEM ADDRESSED] However, for the defective distribution diagram currently disclosed by this invention, differing sharply was proved that it is the created defective distribution diagram (diagram 1 reference) on the basis of the data for which these inventors did experiment * investigation and measured.

Moreover, it became clear that there is an area with high amount of oxygen precipitate and a low area as the N area from which it is distributed over the outer side of the OSF ring.

Therefore, like a conventional method, if the wafer is only manufactured in N area of the OSF ring outer side, N₂ (V) area with many amounts of oxygen precipitate and low N (I) area are intermingled in the wafer, and the device yield was made to reduce from difference of gettering capability.

[0009] This invention was made in view of such a trouble, and neither a V-rich area, nor an I-rich area exists.

When carrying out a heat oxidation treatment, the nucleus of the OSF ring generated in the shape of a ring or OSF ring does not exist.

And, FPD and L/D do not exist over the wafer whole surface.

The crystal whole surface is covered, and while it is extremely low defect density, it aims at obtaining the silicon-single-crystal wafer by the CZ process with the gettering capability by oxygen precipitate, maintaining high-productivity.

[0010]

[SOLUTION OF THE INVENTION] In order to attain the above-mentioned

objective, it succeeded in this invention. In case invention described in Claim 1 of this invention carries out the growth of the silicon single crystal by the Czochralski method, its raising speed is set to $F[\text{mm/min}]$.

When you express the mean value of the gradient degree of crystal inside temperature in the raising axial direction between 1400 degrees C from the melting point of a silicon by $G[\text{degrees C/mm}]$, let distance $D[\text{mm}]$ from the crystal center to the crystal periphery be the horizontal axis.

In the defective distribution diagram (diagram 1 reference) having shown the defective distribution, having used the value of $F/G[\text{mm}^2/\text{degrees C} \cdot \text{min}]$ as the vertical axis, the boundary line of the V-rich area and N1 (V) area, and the boundary line of N1 (V) area and OSF ring area, a crystal is pulled up in N1 (V) area surrounded by this.

It is the manufacturing method of the silicon single crystal characterized by the above-mentioned.

Furthermore as concrete conditions, at the crystal center the above-mentioned value of F/G in the above-mentioned defective distribution diagram, it was presupposed that it pulls up as $0.130 - 0.142 \text{ mm}^2 / \text{degree-C} \cdot \text{min}$ (Claim 2).

[0011] Thus, the pull-up of a crystal in N1 (V) area has narrow area width, as shown in the defective distribution diagram of diagram 1.

Since it applies to the periphery and the suddenly inclines moreover from the crystal center, it is hard to pull up so that the crystal whole surface may be covered and the same area may be secured, and to control conditions.

But, rather than pulling up in the N area of the outer side of the OSF ring area, raising speed can be made quick, and productivity improves.

The silicon-single-crystal wafer with extremely low defect density which enlarged only N1 (V) area to the wafer whole surface as shown in diagram 2 (b) in quality can be obtained.

[0012] And, invention described in Claim 3 of this invention was produced from the silicon single crystal manufactured by the manufacturing method of Claim 1 or Claim 2.

It is the silicon-single-crystal wafer characterized by the above-mentioned.

[0013] Thus the produced silicon-single-crystal wafer is set to the silicon-single-crystal wafer by which the growth was carried out by the Czochralski

method.

When heat oxidation treatment is performed on this wafer whole surface, the nucleus of the OSF ring generated in the shape of a ring or OSF ring does not exist.

And, a V-rich area and an I-rich area do not exist in the so-called wafer whole surface with the wafer for which FPD and L/D(LSEPD, LFPD) do not exist over the wafer whole surface, either.

While it is neutrality (neutral), the precipitate oxygen density (O_i) is high, and gettering capability is large. It is the almost perfect defect-free silicon-single-crystal wafer made only from uniform N1 (V) area, and the device yield can be raised remarkably.

[0014] Hereafter, it demonstrates in detail per this invention.

However, this invention is not limited to these.

In advance of description, lessons are taken from each vocabulary, and it explains beforehand.

With 1) FPD(Flow Pattern Defect), the wafer is cut down from the silicon-single-crystal rod after the growth.

After etching and removing a surface distortion layer with the mixed solution of a hydrofluoric acid and nitric acid, a pit and a ripples pattern arise by etching the surface with the mixed solution of $K_2Cr_2O_7$, hydrofluoric acid, and water (Secco etching), and this ripples pattern is called FPD.

The defect of an oxide-film breakdown-voltage increases so that FPD density within the wafer surface is high (refer Provisional-Publication-No. 4-192345 gazette).

[0015] About 2) SEPD(Secco EtchPit Defect), when giving identical Secco etching as FPD, FPD is that accompanied by flow pattern, and that without flow pattern is called SEPD.

It is considered that large SEPD (LSEPD) 10 micrometres or more originates in the transition cluster in this.

When the transition cluster exists in the device, electricity leaks through this transition, and it stops achieving the function as P-N junction.

[0016] With 3)LSTD(Laser Scattering Tomography Defect), a wafer is cut down from the silicon-single-crystal rod after growth.

The wafer is opened after etching and removing the surface distortion layer with the mixed solution of hydrofluoric acid and nitric acid.

Infrared-light is incidented on this cleavage plane.

The scattered light by the defect which exists in the wafer by detecting the light which came out from the wafer surface is detectable.

About the dispersion object observed here, at conferences etc., there is already a report.

Refer to (J.J.A.P. Vol.32, P3679,1993 it is considered that it is oxygen deposit).

Moreover, the result referred to as being the void (hole) of an octahedron is also reported by the latest study.

[0017] 4)COP(Crystal Originated Particle) is the defect which degrades the oxide-film breakdown-voltage of the main part of a wafer.

The defect becoming FPD in Secco etch works as selective etching liquid in the cleaning by the ammonia hydrogen-peroxide-solution cleaning ($\text{NH}_4\text{OH}:\text{H}_2\text{O}_2:\text{H}_2\text{O}=1:1:10$ mixed solution, it becomes COP.

The diameter of this pit is investigated by the light scattering measurement at 1 micrometre or less.

[0018] 5) LSEPD and LFPD etc. in L/D (abbreviation of the transition loop between Large Dislocation: lattices).

It is the defect considered to be caused by transition loop.

For LSEPD also in SEPD, as described above, that 10 micrometres or larger is referred to.

Moreover, for FPD which is LFPD described above, that 10 micrometres or larger is said, and being caused by transition loop is considered also here.

[0019] These inventor, related with the silicon single crystal growth by the CZ process, as previously proposed in unexamined Japanese patent 9-199415, it becomes as follows.

About the limit neighborhood of V area and I area, when investigating in detail, FPD, LSTD, COP number is remarkably low in the extremely narrow area of this limit neighborhood, and it was discovered that there was a neutral area where LSEPD does not exist, either.

[0020] Then, when this neutral area could be extended to the wafer whole surface, it was conceived that point defects could be reduced sharply.

Namely, in the relationship of growth (raising) speed and temperature gradient, for the horizontal direction of the crystal, namely, in the wafer plane, since raising speed is almost fixed, the main factors which decide the density distribution of the in-plane point defect are temperature gradients.

In other words in the wafer plane, it is a problem that there is a difference in the temperature gradient in the axial direction. If this difference can be reduced, it will be discovered that the density difference of the point defect within the wafer surface can also be reduced.

Temperature in the furnace is controlled to set the difference of the temperature gradient G_c of the in-crystal centre part, and temperature-gradient G_e of the crystal periphery part to $(\Delta)G = (G_e - G_c) \leq 5$ degrees C/cm.

When raising speed was adjusted, the wafer without the defect with the wafer whole surface made from N area can be obtained.

[0021] With this invention, difference $(\Delta)G$ of the above temperature gradients uses the crystal drawing apparatus by the small CZ process.

Raising speed was changed and the inside of a crystal plane was investigated.

As a result, the following two realisations were obtained newly.

These inventors experimented * investigated.

N area which exists between the V-rich area and the I-rich area as a result is the outer side of the OSF ring (nucleus) conventionally. [N (I) area is referred to hereafter, diagram 2(a) reference] only this was considered.

However, it was confirmed that N area existed also inside the OSF ring. [below, called N1 (V) area. Diagram 2(a) reference]

In namely, the case of the above-mentioned unexamined Japanese patent 9-199415, the OSF ring, it had become the boundary between V-rich area and N area. (Refer diagram 3 (a)) It was found that these two are not necessarily in agreement.

[0022] As another discovery, in the N area of the outer side of the OSF ring area, the area with high oxygen precipitate and low area exists, and it turned out that there is high oxygen precipitate in the inner side adjoining the OSF ring area.

Namely, N area by the side of V whose I which adjoins the outer side of the OSF ring is not rich. [N2 (V) area is called hereafter.] It has turned out that this exists.

[Refer to diagram 1 and diagram 2 (a).]

[0023] Therefore, like the process disclosed by the above-mentioned Provisional-Publication-No. 8-330316 gazette, if the wafer is produced only in N area of the OSF ring outer side, it is clear that the wafer whole surface is N area.

However, a difference arises in oxygen precipitate on the inner side and the outer side of a wafer.

The wafer with which in-plane gettering capability differs will be made.

Incidentally, there is high oxygen precipitate and N2 (V) area of the inner side which adjoins OSF ring area having gettering capability sufficiently.

N (I) area by the side of an I-rich area has low oxygen precipitate, and its gettering capability is low.

[0024] Then, as shown in the defective distribution diagram of diagram 1, it is ideal to produce the wafer of only N1 (V) area which is a whole-surface N area adjoining inside OSF ring area, and the almost perfect defect-free silicon single crystal can be obtained.

[Refer to diagram 2 (a) and (b).] However, the area is very narrow.

And, since it is the area which is going abruptly up in the radial direction position of a crystal, in order to control to adjust raising speed F and temperature-gradient G , and to fit the value of F/G in this area, it is accompanied by remarkable difficulty.

However, the pull-up of the crystal is possible.

Instead of pulling up in N area of the outer side of the OSF ring area, since raising speed can be made quick, productivity improves.

[0025] For temperature of the raising apparatus in this investigation in the furnace comprehensive heat-transfer analysis, using soft(ware), FEMAG(F.Dupret, P.Nicodeme, Y.Ryckmans, P.Wouters, and M.J.Crochet, Int.J.Heat Mass Transfer,33,1849(1990)), it was analyzed zealously using this.

As a result, raising speed is set to $F[\text{mm/min}]$.

It is G the mean value of the gradient degree of crystal inside temperature in the

raising axial direction between 1400 degrees C from the melting point of a silicon.

When expressing this with [degrees C/mm], it is a pull-up in N1 (V) area.

The value of F/G is within the limits of 0.130 - 0.142 mm² / degree-C *min at the crystal center, if raising speed F and temperature-gradient mean-value G are controlled and a crystal is pulled up, the silicon single crystal without a crystal defect is obtained.

[0026] Diagram 1 makes a horizontal axis the radial direction position (diameter of 6 inches) of a crystal.

The various defects distribution at the time of making F/G value into the vertical axis is expressed.

For the limit of the V-rich area /N1 (V) area, as shown clearly from diagram 1, it raises gently from 0.142 mm² / degree-C *min between the crystal-center position and the position from the center to about 50 mm.

On the line which increased F/G value abruptly, from this position to the periphery, the center of the OSF ring area is about 0.125 mm² / degree-C *min, and is applied to the crystal periphery.

The boundary line of an OSF ring area /N2 (V) area is also mostly parallel, and the boundary line of N1 (V) area / OSF ring area also raises gently.

On the line which increased F/G value abruptly from 65 mm from the crystal-center position to the periphery, moreover, the boundary line with N(I) area / I-rich area becomes about 0.112 - 0.117 mm² / degree-C *min between the crystal-center position and the position from the center to about 60 mm.

Then, it falls abruptly toward the crystal periphery.

In order to follow and to utilize fully N1 (V) area except the area of the outer side of the V-rich area in a wafer, and OSF ring area, what is sufficient is just to control F and G so that F/G value becomes 0.130 - 0.142 mm² / degree-C *min at the crystal-center position.

[0027] Demonstrating from the viewpoint of the wafer, conventionally, as shown in diagram 3 (a), for usual raising speed and usual crystal drawing apparatus, n area which exists in the outer side of the OSF ring should enlarge to the crystal whole surface.

[Refer diagram 3 (b).]It pulls up using a special crystal drawing apparatus, and speed and G (delta-symbol) are controlled.

In this way, it can manufacture the defect-free crystal.

However, the control range of manufacture conditions, such as raising speed and the temperature gradient, is very narrow, control is difficult and there is difficulty in productivity, and it was not practical.

In the N area which exists in the outer side of the OSF ring on it, in the inner side adjoining the OSF ring area, there is an area (N2 (V)) area with high oxygen precipitate.

Since the low area (N (I) area) of oxygen precipitate exists in the outer side, if a wafer is produced only in the N area of the OSF ring outer side, it is clear that the wafer whole surface is N area.

However, a difference arises in oxygen precipitate on the inner side and the outer side of a wafer.

The wafer with which in-plane gettering capability differs will be made.

[0028] When limiting only to N1 (V) area inside OSF ring discovered this time, with this invention [Refer to diagram 2 (a) and (b).] It will pull up in the narrow area.

Although the control of raising conditions is not easy, the pull-up of the crystal is possible.

The extremely high quality wafer of a whole-surface N area is producible with extremely low defect density with gettering capability as mentioned above.

In this case, as mentioned above, since a control range is narrow with this invention, OSF may occur in the periphery part of the raising single-crystal rod.

However, since OSF of the periphery part of a raising single-crystal rod is eliminated in a single-crystal rod after that in case it is sliced and processed into a wafer, and cylindrical grinding, it is satisfactory.

[0029]

[Embodiment] Hereafter, the embodiment of this invention is demonstrated in detail, referring to drawings.

First, diagram 5 demonstrates the example of composition of the single crystal drawing apparatus by the CZ process used with this invention.

As shown in diagram 5, for this single crystal drawing apparatus 30, raising chamber 31, the crucible 32 provided in the raising chamber 31, the heater 34 configured around a crucible 32, the crucible maintenance axis 33 which rotates

a crucible 32, and the rotating mechanism (not shown), the seed chuck 6 holding the seed crystal 5 of silicon, the coiling device which rotates or rolls the cable 7 which pulls up the seed chuck 6, and the cable 7 (not shown), it has these and it is constituted.

A quartz crucible is provided to the side in which a crucible 32 accommodates silicon melt solution (melt) 2 inside.

The graphite crucible is provided on the outer side.

Moreover, the heat insulating material 35 is configured around the outer side of heater 34.

[0030] Moreover, in order to set up the manufacture conditions in connection with the manufacturing method of this invention, the cyclic solid-liquid boundary-surface heat insulating material 8 is provided on the periphery of the solid-liquid boundary surface of the crystal.

Above this, the upper surrounding heat insulating material 9 is situated.

This solid-liquid boundary-surface heat insulating material 8 provides the 3-5-cm gap 10 between the lower end and the melt surface of the silicon melt solution 2, and is installed between.

The upper surrounding heat insulating material 9 may not be used according to conditions.

Furthermore, cooling gas is sprayed in.

Moreover, the cylindrical cooling system 36 which blocks the radiant heat and cools the single crystal is provided.

Independently, recently, the magnet which is pulled up and is not illustrated on the horizontal outer side of chamber 31 is installed.

The convection current of melt solution is suppressed by applying the magnetic field of a horizontal direction or perpendicularly directional etc. to the silicon melt solution 2.

This so-called MCZ method which aims at stable growth of a single crystal is used in many cases.

[0031] Next, the single-crystal cultivation method by the above-mentioned single crystal drawing apparatus 30 is demonstrated.

First, the high-purity polycrystal raw material of silicon is heated and fused within crucible 32 beyond the melting point (about 1420 degrees C).

Next, the surface roughly center part of melt solution 2 is made to contact or

immerse the end of seed crystal 5 by starting rolling cable 7.

Then, a single crystal growth is started by rolling up, rotating cable 7, while rotating the crucible maintenance axis 33 in the proper direction, and pulling up seed crystal 5.

Henceforth, the single-crystal rod 1 of a roughly cylinder shape can be obtained by adjusting raising speed and temperature pertinently.

[0032] In this case, with this invention, it was shown in diagram 5 that it is important especially in order to attain the objective of this invention.

In the periphery space of the liquefied part in the single-crystal rod 1 on the molt surface of the raising chamber 31, the temperature of the crystal near the molt surface is a temperature region from 1420 degrees C to 1400 degrees C, in this range, the cyclic solid-liquid boundary-surface heat insulating material 8 was provided, It is having situated on it the upper surrounding heat insulating material 9.

Furthermore, the apparatus 36 which cools the crystal, for example, cooling system, is provided on the upper part of this heat insulating material depending on the need.

Cooling gas shall be sprayed on this from the upper part, and the crystal shall be cooled.

It is good also as structure which installed the radiant-heat reflecting plate in the tube lower part.

[0033] Thus predetermined gap is provided to the position directly above molt surface, and a heat insulating material is configured.

Furthermore by considering as the structure which provided the apparatus which cools a crystal to the upper part of this heat insulating material, a heat-retention effect is obtained by the radiant heat near the crystal-growth boundary surface.

Since the radiant heat from the heater etc. can be blocked, the manufacture conditions of this invention can be satisfied in the upper part of the crystal.

As a cooling system of this crystal, separate from the above-mentioned cylindrical cooling system 36, the air-cooling duct, the water-cooled coil, etc. which surround the perimeter of the crystal are provided, and it may be made to secure the desired temperature gradient.

[0034] The single crystal drawing apparatus used with this invention and the apparatus conventional for comparison are shown in diagram 6.

About the fundamental structure, it is the same as that of the raising apparatus used with this invention.

However, neither the solid-liquid boundary-surface heat insulating material 8, the upper surrounding heat insulating material 9 nor the cooling system 36 is equipped.

[0035]

[Embodiment] Hereafter, an embodiment is given and the concrete embodiment of this invention is demonstrated.

However, this invention is not limited to these.

(Embodiment 1)

With the raising apparatus 30 shown in diagram 5, 60kg charge of the raw-material polycrystal silicon is carried out in a 20 inch quartz crucible.

The diameter of 6 inches and the silicon-single-crystal rod of a bearing <100> were changed to 0.88 - 0.50 mm/min mean raising speed and was pulled up (the straight cylinder length of about 85 cm of a single-crystal rod).

The hot-water temperature of silicon melt solution is about 1420 degrees C, and the lower end of the circular solid-liquid boundary-surface heat insulating material is 4-cm separated from melt surface.

The circular solid-liquid boundary-surface heat insulating material of 10 cm height is situated on it.

It pulls up from melt surface, and a crucible maintenance axis is adjusted and height to the chamber ceiling is set to 30 cm.

The upper surrounding heat insulating material was arranged.

And, F/G value in the in-crystal centre part was changed to 0.22 - 0.10 mm² * degrees C/min, and it was pulled up.

[0036] The wafer is cut down from the single-crystal rod obtained here.

A mirror-surface process is applied and the mirror-surface wafer of a silicon single crystal is produced.

The grown-in defect was measured.

Moreover, the heat oxidation treatment was given and existence of the OSF ring generating was confirmed.

As a result, F/G value within the range of 0.130 - 0.142 mm² / degree-C *min at the crystal center, the extremely low defect wafer for which N1 (V) area was enlarged as much as possible was obtained.

In addition, the oxide-film breakdown-voltage characteristic of this wafer became 100% C-mode rate, an excellent article.

In addition, C-mode measurement conditions are as follows.

1) oxide-film:25 nm, 2) Measurement electrode: phosphorus dope * polysilicon, 3) Electrode area:8 mm², 4) evaluation current :1mA/cm², 5) excellent-article standard: That whose dielectric-breakdown electric field is 8MV/ cm or greater was judged to be an excellent article.

[0037] In addition, this invention is not limited to the above-mentioned embodiment.

The above-mentioned embodiment is an illustration.

It has the same composition substantially with the technical thought described by the claim of this invention.

For that having the same effect, it is included by the technical range of this invention in all cases.

[0038] For example, in the above-mentioned embodiment, when the silicon single crystal with a diameter of 6 inches was grown, the example was given and demonstrated.

However, this invention is not limited to this and raising speed is set to F[mm/min].

It is G the mean value of the gradient degree of crystal inside temperature in the raising axial direction between 1400 degrees C from the melting point of a silicon.

If a crystal is pulled up in N1 (V) area which exists inside OSF ring area in the above-mentioned defective distribution diagram when expressed with [degrees C/mm], regardless of diameter, for example, it is applicable also to the silicon single crystal of the diameter of 8-16 inches, or more.

Moreover, this invention impresses a horizontal magnetic field, a longitudinal magnetic field, a cusp magnetic field, etc. to the silicon melt solution. It is needless to say that it is applicable also to this so-called MCZ method.

[0039]

[EFFECT OF THE INVENTION] As explained above, according to this invention, neither a V-rich area, nor an I-rich area exists in the whole-surface N1 (V) area.

When carrying out a heat oxidation treatment, the nucleus of the OSF ring generated in the shape of a ring or OSF ring does not exist.

And, FPD and L/D do not exist over the wafer whole surface.

Over the crystal whole surface, and while it has extremely low defect density, the silicon-single-crystal wafer by the CZ process with the gettering capability by oxygen precipitate can be manufactured, maintaining high-productivity.

[BRIEF EXPLANATION OF DRAWINGS]

[FIGURE 1] Let the radial direction position of the crystal within the silicon-single-crystal wafer surface discovered with this invention be a horizontal axis.

It shows various defects distribution in the diagram at the time of making F/G value into the vertical axis.

[FIGURE 2] An explanatory drawing showing various defects distributions in a crystal plane discovered with this invention.

(a) When pulling up under usual raising conditions, (b) When pulling up on the specific raising conditions of this invention.

[FIGURE 3] An explanatory drawing showing the many defects distribution in a crystal plane in the conventional process for raising.

(a) When pulling up under usual raising conditions, (b) When the raising speed and the gradient degree of crystal inside temperature was precisely controlled and it was pulled up.

[FIGURE 4] The explanatory drawing which expressed the relationship with a defective distribution in the raising speed in the conventional process to pull up, and the crystal plane.

(a) In the case of a high-speed pull-up (b) In the case of a medium-speed pull-up (c) In the case of a low-speed pull-up

[FIGURE 5] The schematic explanatory drawing of the single crystal drawing

apparatus by the CZ process used with this invention.

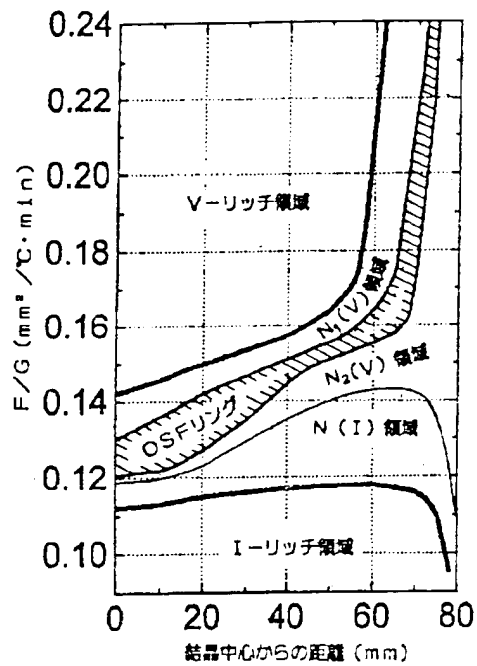
[FIGURE 6] The schematic explanatory drawing of the conventional single crystal drawing apparatus by the CZ process.

[EXPLANATION OF DRAWING]

1... growth single-crystal rod, 2... silicon melt solution, 3... melt surface, 4... solid-liquid boundary surface, 5... seed crystal, 6... seed chuck, 7... cable, 8... solid-liquid boundary-surface heat insulating material, 9... upper surrounding heat insulating material, 10...gap between melt surface and the solid-liquid boundary-surface heat-insulating-material lower end, 30... Single crystal drawing apparatus, 31... raising chamber, 32... crucible, 33... crucible maintenance axis, 34... heater, 35... heat insulating material, 36... cooling system.

V...V- rich area, n...N- area, n1 (V)...N1 (V) area, n2 (V)...N2 (V) area, n(l)...N(l) area, l...l- rich area, OR...OSF ring.

[FIGURE 1]

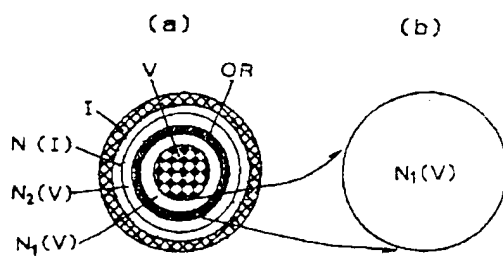


[translation of Japanese text in Figure 1]

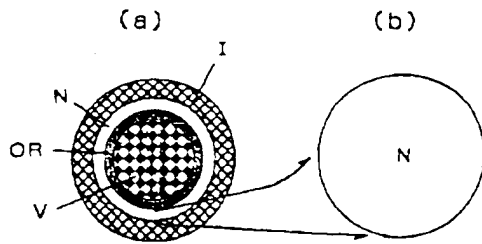
horizontal axis: distance (mm) from crystal center

regions from top to bottom: V-rich region, $N_1(V)$ region, OSF ring, $N_2(V)$ region, $N(I)$ region, I-rich region

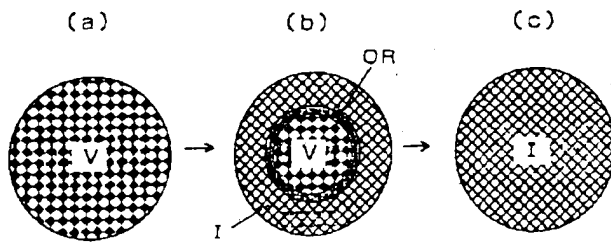
[FIGURE 2]



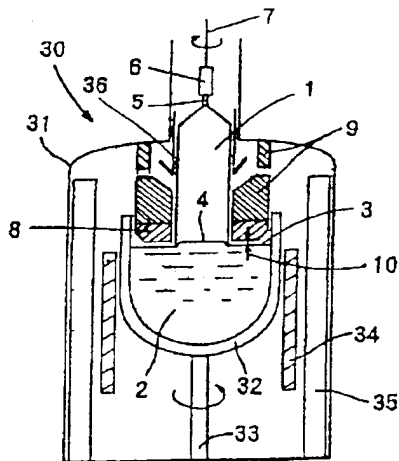
[FIGURE 3]



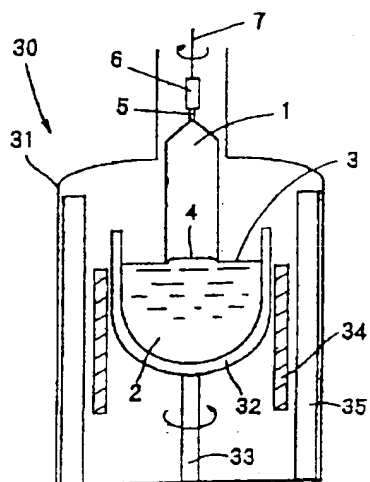
[FIGURE 4]



[FIGURE 5]



[FIGURE 6]



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